ABSTRACT OF THE DISCLOSURE

A power-on reset circuit is capable of outputting a normal reset signal despite slow rise of power supply voltage. A node is interposed between a MOS capacitor including a PMOS with its drain and source connected in common and an NMOS having its gate fixedly connected to a ground potential. The node is connected to a ground potential via the NMOS and also to a power supply line via the MOS capacitor. Therefore, even when the power supply voltage rises slowly after power is turned on, the potential of the node rises substantially at the same rate as the power supply voltage. After the power supply voltage reaches a predetermined power supply potential, the potential of the node is gradually lowered due to an off leakage current through the NMOS. The node is connected with an inverter operating according to the power supply voltage. When the potential of the node decreases below 1/2 of the power supply voltage, the reset signal outputted from the inverter goes to the H level.